



M68AF031AL

256 Kbit (32K x 8) 5.0V Asynchronous SRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 4.5 to 5.5V
- 32K x 8 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIME: 70ns
- LOW STANDBY CURRENT
- LOW V_{CC} DATA RETENTION: 2V
- TRI-STATE COMMON I/O
- AUTOMATIC POWER DOWN

Figure 1. Packages

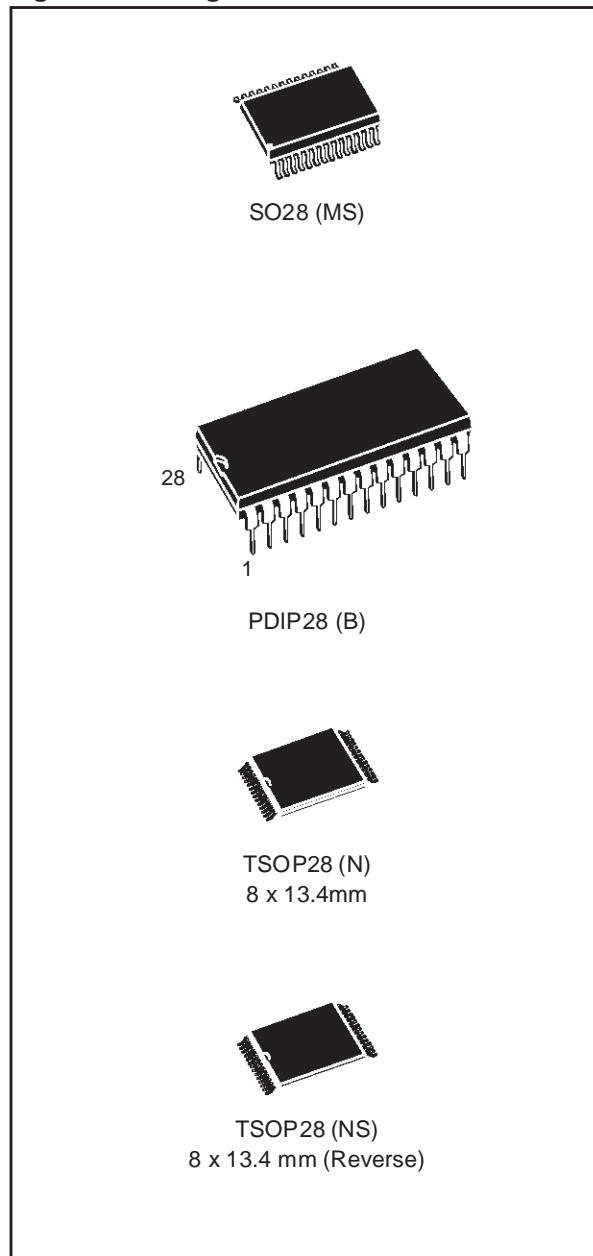


TABLE OF CONTENTS

SUMMARY DESCRIPTION. 3

- Figure 2. Logic Diagram 3
- Table 1. Signal Names 3
- Figure 3. SO Connections 4
- Figure 4. DIP Connections 4
- Figure 5. TSOP Connections (Normal) 4
- Figure 6. TSOP Connections (Reverse) 4
- Figure 7. Block Diagram 5

MAXIMUM RATING. 5

- Table 2. Absolute Maximum Ratings. 5

DC AND AC PARAMETERS. 6

- Table 3. Operating and AC Measurement Conditions. 6
- Figure 8. AC Measurement I/O Waveform 6
- Figure 9. AC Measurement Load Circuit 6
- Table 4. Capacitance. 7
- Table 5. DC Characteristics. 7

OPERATION 8

- Table 6. Operating Modes. 8
- Read Mode 8
- Figure 10. Address Controlled, Read Mode AC Waveforms. 8
- Figure 11. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms. 9
- Figure 12. Chip Enable Controlled, Standby Mode AC Waveforms 9
- Table 7. Read and Standby Mode AC Characteristics 10
- Write Mode 11
- Figure 13. Write Enable Controlled, Write AC Waveforms 11
- Figure 14. Chip Enable Controlled, Write AC Waveforms. 12
- Table 8. Write Mode AC Characteristics 13
- Figure 15. Low V_{CC} Data Retention AC Waveforms 14
- Table 9. Low V_{CC} Data Retention Characteristics. 14

PACKAGE MECHANICAL 15

- SO28 - 28 lead Plastic Small Outline, 300 mils body width, Package Outline 15
- SO28 - 28 lead Plastic Small Outline, 300 mils body width, Package Mechanical Data 15
- PDIP28 - 28 pin Plastic DIP, 600 mils width, Package Outline 16
- PDIP28 - 28 pin Plastic DIP, n600 mils width, Package Mechanical Data 16
- TSOP28 - 28 lead Normal and Reverse Pinout Plastic Small Outline, Package Outline 17
- TSOP28 - 28 lead Normal and Reverse Pinout Plastic Small Outline, Package Mechanical Data. 17

PART NUMBERING 18

- Table 13. Ordering Information Scheme 18

REVISION HISTORY. 19

- Table 14. Document Revision History 19

SUMMARY DESCRIPTION

The M68AF031AL is a 256 Kbit (262,144 bit) CMOS SRAM, organized as 32,768 bytes. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 4.5 to 5.5V supply. This device has an automatic power-

down feature, reducing the power consumption by over 99% when deselected.

The M68AF031AL is available in SO28 (28-lead Small Outline), PDIP28 (28-pin Plastic Dual-In-Line) and TSOP28 (28-lead Thin Small Outline, Standard and Reverse Pinout) packages.

Figure 2. Logic Diagram

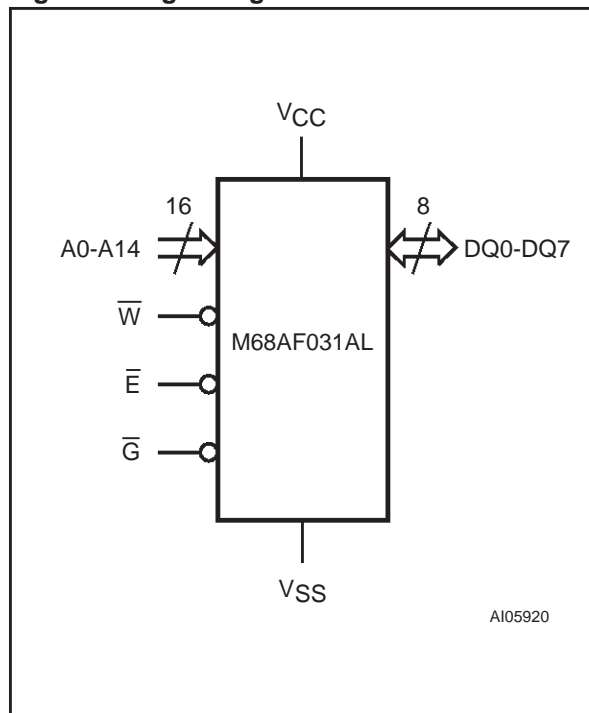


Table 1. Signal Names

A0-A14	Address Inputs
DQ0-DQ7	Data Input/Output
\bar{E}	Chip Enable
\bar{G}	Output Enable
\bar{W}	Write Enable
VCC	Supply Voltage
VSS	Ground
NC	Not Connected Internally

M68AF031AL

Figure 3. SO Connections

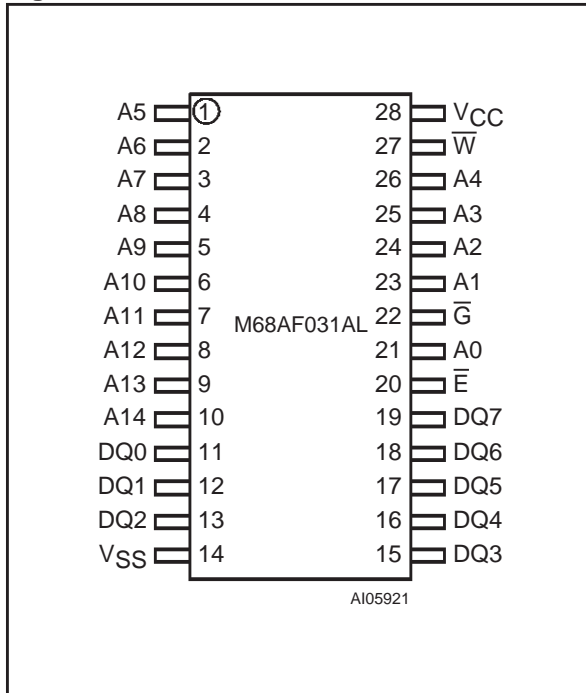


Figure 5. TSOP Connections (Normal)

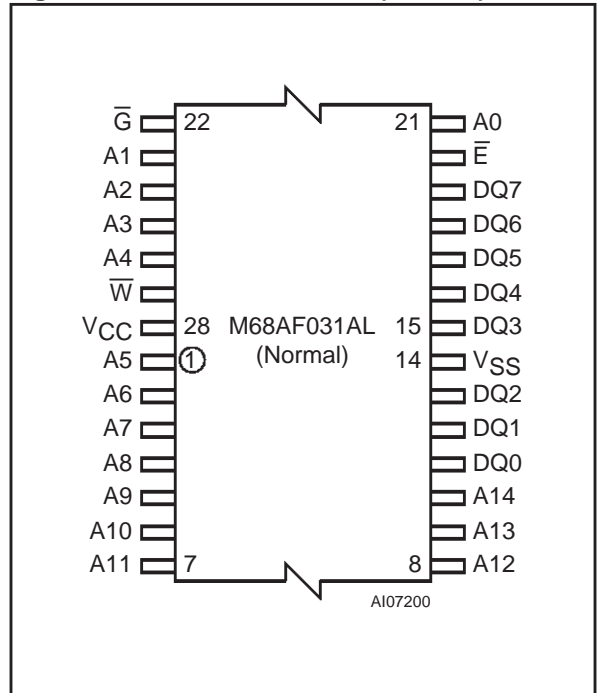


Figure 4. DIP Connections

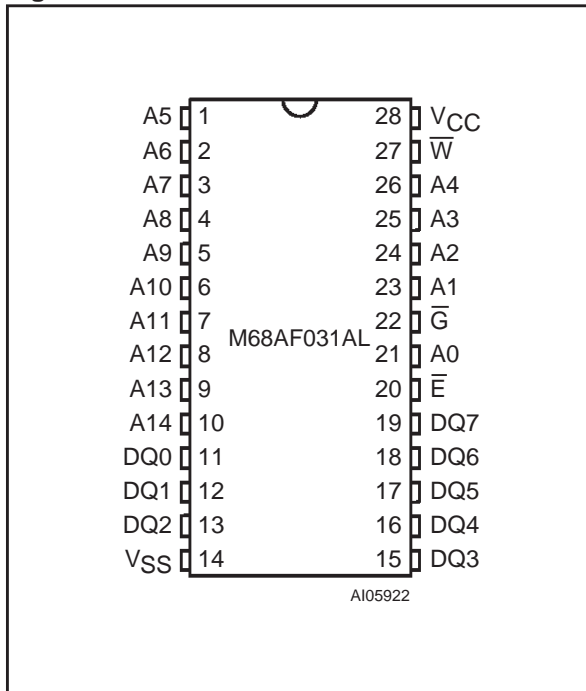


Figure 6. TSOP Connections (Reverse)

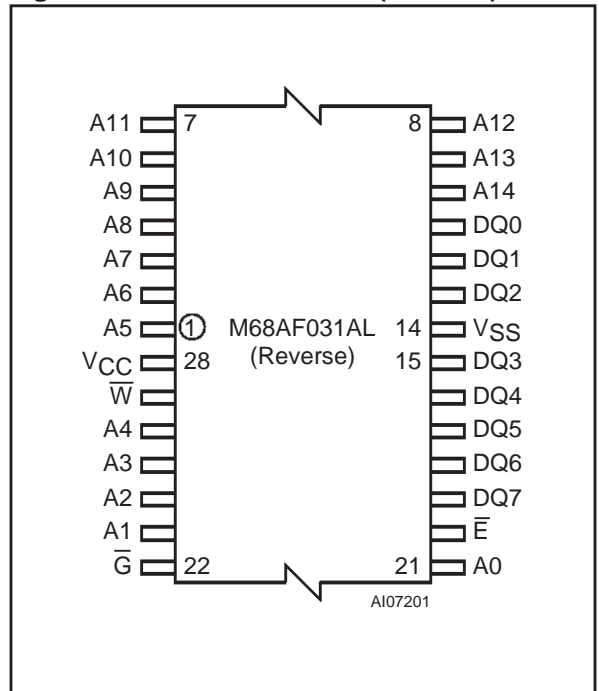
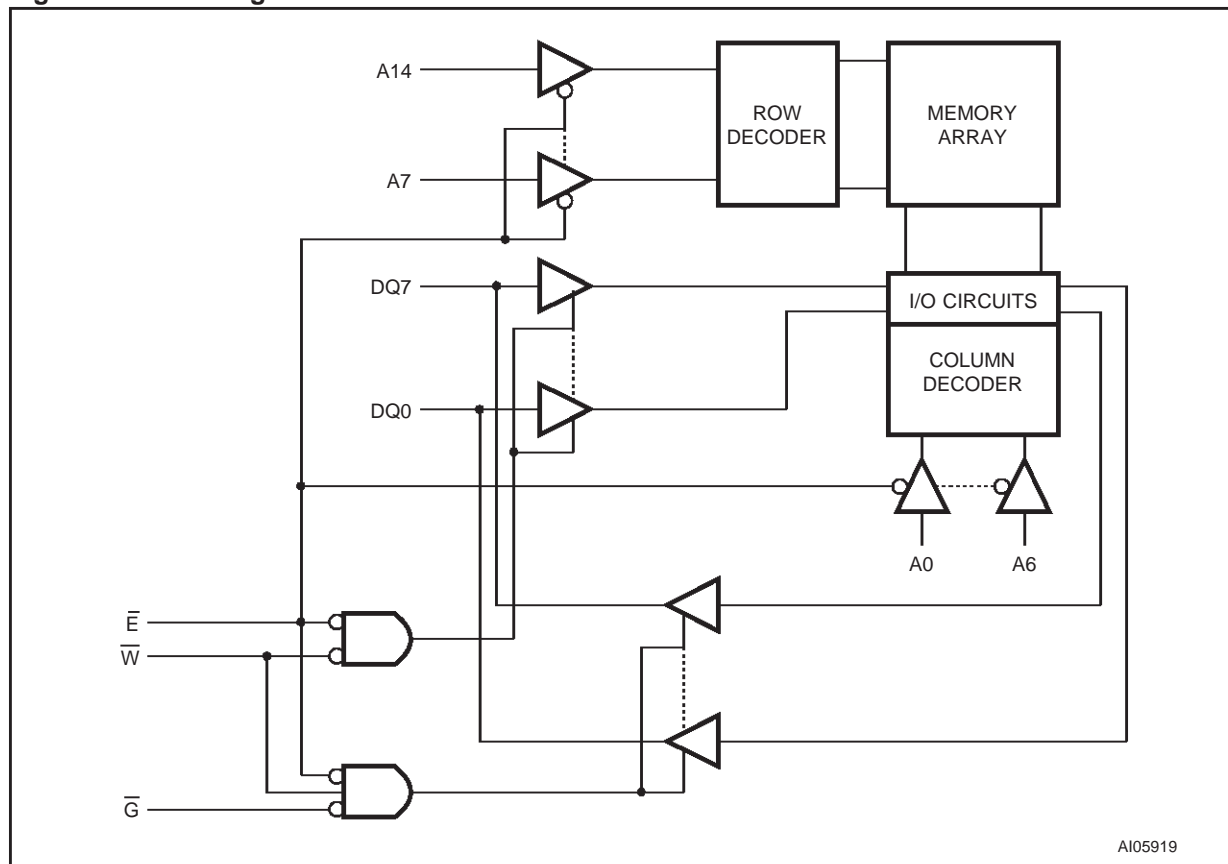


Figure 7. Block Diagram



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MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not im-

plied. Exposure to Absolute Maximum Rating conditions for periods greater than 1 sec periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$I_O^{(1)}$	Output Current	20	mA
P_D	Power Dissipation	1	W
T_A	Ambient Operating Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 150	°C
V_{CC}	Supply Voltage	-0.5 to 6.5	V
$V_{IO}^{(2)}$	Input or Output Voltage	-0.5 to $V_{CC} + 0.5$	V

Note: 1. One output at a time, not to exceed 1 second duration.
2. Up to a maximum operating V_{CC} of 6.0V only.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

Parameter		M68AF031AL
V _{CC} Supply Voltage		4.5 to 5.5V
Ambient Operating Temperature	Range 1	0 to 70°C
	Range 6	-40 to 85°C
Load Capacitance (C _L)		100pF
Output Circuit Protection Resistance (R ₁)		3.0kΩ
Load Resistance (R ₂)		3.1kΩ
Input and Output Timing Ref. Voltages		V _{CC} /2
Input Rise and Fall Times		1ns/V
Input Pulse Voltages		0 to V _{CC}
Output Transition Timing Ref. Voltages		V _{RL} = 0.3V _{CC} ; V _{RH} = 0.7V _{CC}

Figure 8. AC Measurement I/O Waveform

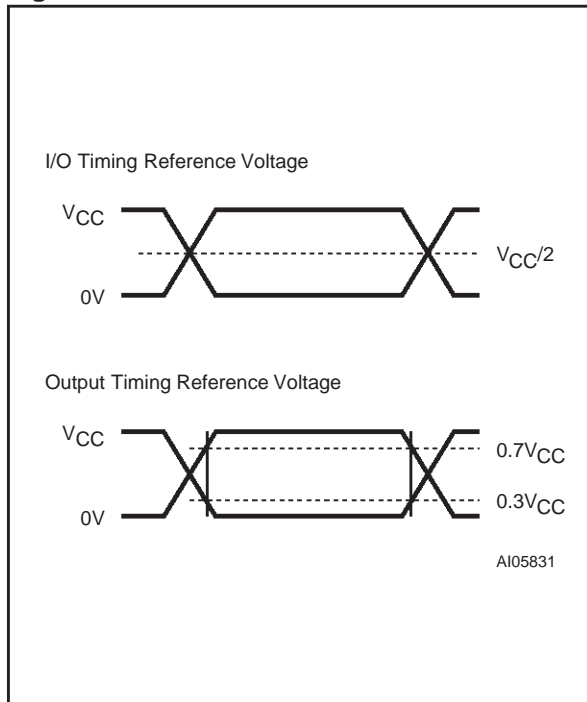


Figure 9. AC Measurement Load Circuit

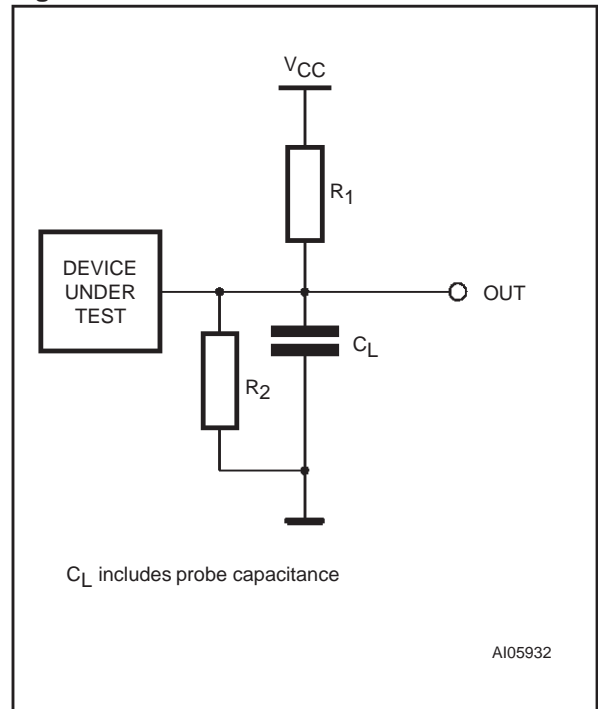


Table 4. Capacitance

Symbol	Parameter ^(1,2)	Test Condition	Min	Max	Unit
C _{IN}	Input Capacitance on all pins (except DQ)	V _{IN} = 0V		6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V		8	pF

Note: 1. Sampled only, not 100% tested.
2. At T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I _{CC1} ^(1,2)	Operating Supply Current	V _{CC} = 5.5V, f = 1/t _{AVAV} , I _{OUT} = 0mA			50	mA
I _{CC2} ⁽³⁾	Operating Supply Current	V _{CC} = 5.5V, f = 1MHz, I _{OUT} = 0mA			5	mA
I _{SB}	Standby Supply Current CMOS	V _{CC} = 5.5V, f = 0, E ≥ V _{CC} - 0.2V	Range 1	0.1	5	μA
			Range 6	0.1	10	μA
I _{LI}	Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	-1		1	μA
I _{LO} ⁽⁴⁾	Output Leakage Current	0V ≤ V _{OUT} ≤ V _{CC}	-1		1	μA
V _{IH}	Input High Voltage		2.2		V _{CC} + 0.3	V
V _{IL}	Input Low Voltage		-0.3		0.8	V
V _{OH}	Output High Voltage	I _{OH} = -1.0mA	2.4			V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA			0.4	V

Note: 1. Average AC current, cycling at t_{AVAV} minimum.
2. E = V_{IL}, V_{IN} = V_{IL} OR V_{IH}.
3. E ≤ 0.2V, V_{IN} ≤ 0.2V OR V_{IN} ≥ V_{CC} - 0.2V.
4. Output disabled.

M68AF031AL

OPERATION

The M68AF031AL has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted (\bar{E} = High). An Output Enable (\bar{G}) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

Operational modes are determined by device control inputs \bar{W} and \bar{E} , as summarized in the Operating Modes table (see Table 6).

Table 6. Operating Modes

Operation	\bar{E}	\bar{W}	\bar{G}	DQ0-DQ7	Power
Deselected	V_{IH}	X	X	Hi-Z	Standby (I_{SB})
Read	V_{IL}	V_{IH}	V_{IL}	Data Output	Active (I_{CC})
Write	V_{IL}	V_{IL}	X	Data Input	Active (I_{CC})
Output Disabled	V_{IL}	V_{IH}	V_{IH}	Hi-Z	Active (I_{CC})

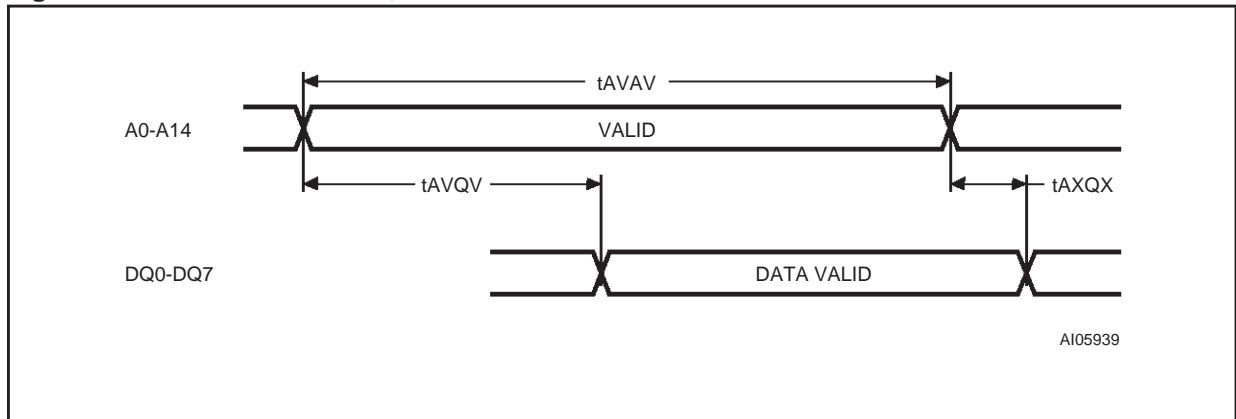
Note: 1. X = V_{IH} or V_{IL} .

Read Mode

The M68AF031AL is in the Read mode whenever Write Enable (\bar{W}) is High with Output Enable (\bar{G}) Low, and Chip Enable (\bar{E}) is asserted. This provides access to data of the 262,144 locations in the static memory array, specified by the 15 address inputs. Valid data will be available at the eight output pins within t_{AVQV} after the last stable

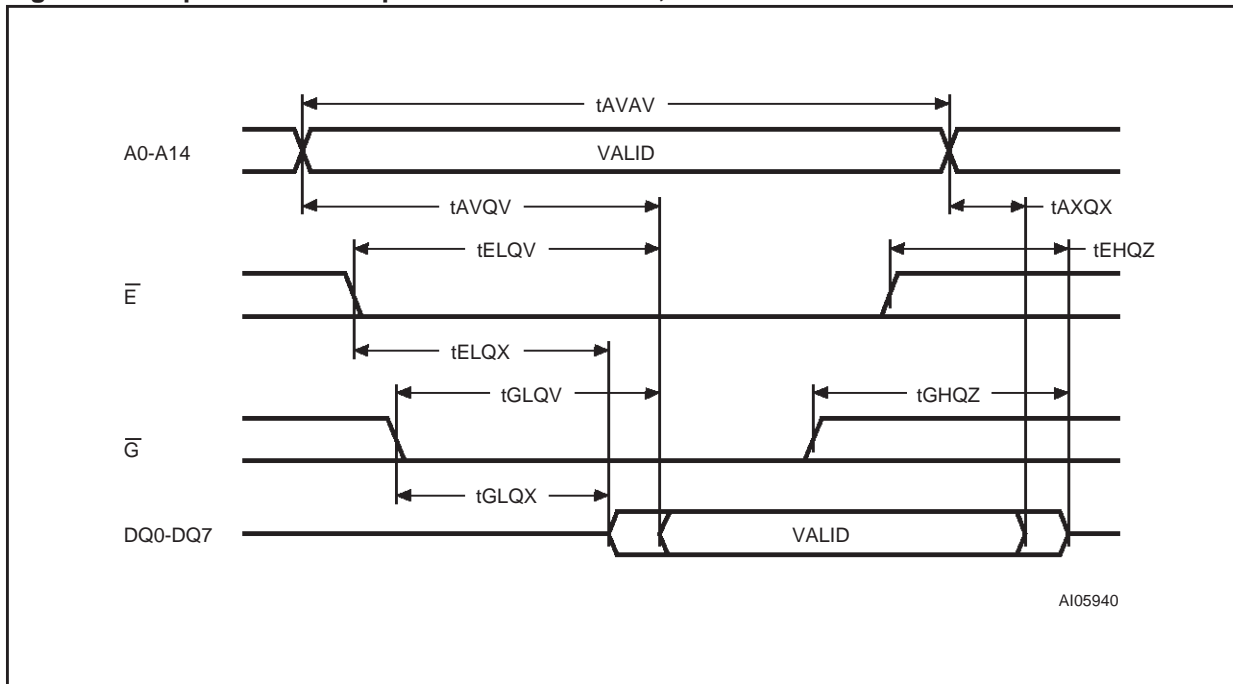
address, providing \bar{G} is Low and \bar{E} is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX} and t_{GLQX} but data lines will always be valid at t_{AVQV} .

Figure 10. Address Controlled, Read Mode AC Waveforms



Note: \bar{E} = Low, \bar{G} = Low, \bar{W} = High.

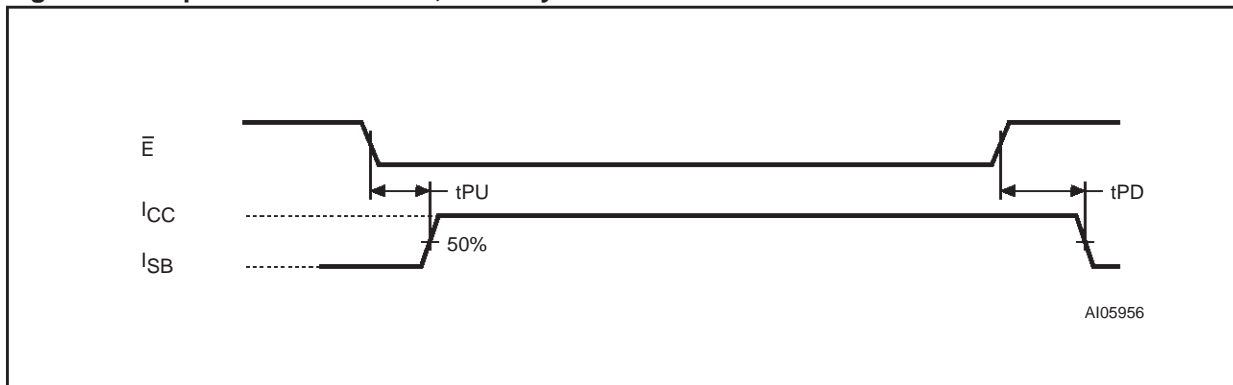
Figure 11. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.



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Note: Write Enable (\bar{W}) = High.

Figure 12. Chip Enable Controlled, Standby Mode AC Waveforms



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Table 7. Read and Standby Mode AC Characteristics

Symbol	Parameter		M68AF031AL	Unit
			70	
t_{AVAV}	Read Cycle Time	Min	70	ns
t_{AVQV}	Address Valid to Output Valid	Max	70	ns
$t_{AXQX}^{(1)}$	Data hold from address change	Min	10	ns
$t_{EHQZ}^{(2,3)}$	Chip Enable High to Output Hi-Z	Max	25	ns
t_{ELQV}	Chip Enable Low to Output Valid	Max	70	ns
$t_{ELQX}^{(1)}$	Chip Enable Low to Output Transition	Min	10	ns
$t_{GHQZ}^{(2,3)}$	Output Enable High to Output Hi-Z	Max	25	ns
t_{GLQV}	Output Enable Low to Output Valid	Max	35	ns
$t_{GLQX}^{(1)}$	Output Enable Low to Output Transition	Min	5	ns
$t_{PD}^{(4)}$	Chip Enable High to Power Down	Max	0	ns
$t_{PU}^{(4)}$	Chip Enable Low to Power Up	Min	70	ns

Note: 1. Test conditions assume transition timing reference level = $0.3V_{CC}$ or $0.7V_{CC}$.

2. At any given temperature and voltage condition, t_{GHQZ} is less than t_{GLQX} and t_{EHQZ} is less than t_{ELQX} for any given device.

3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

4. Tested initially and after any design or process changes that may affect these parameters.

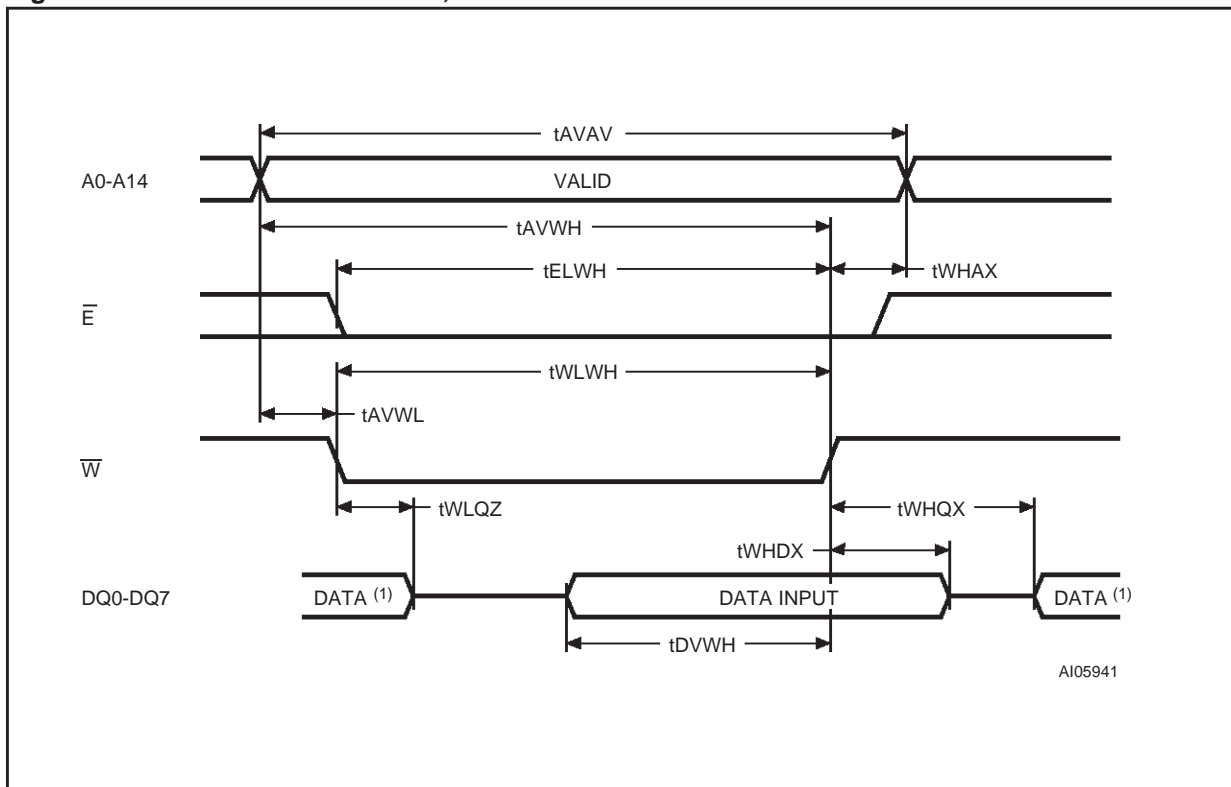
Write Mode

The M68AF031AL is in the Write mode whenever the \overline{W} and \overline{E} are Low. Either the Chip Enable input (\overline{E}) or the Write Enable input (\overline{W}) must be deasserted during Address transitions for subsequent write cycles. When \overline{E} (\overline{W}) is Low, write cycle begins on the \overline{W} (\overline{E})'s falling edge. Therefore, address setup time is referenced to Write Enable or Chip Enable as t_{AVWL} and t_{AVEL} respectively, and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of \overline{E} or \overline{W} .

If the Output is enabled ($\overline{E} = \text{Low}$, $\overline{G} = \text{Low}$), then \overline{W} will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of \overline{E} , whichever occurs first, and remain valid for t_{WHDX} and t_{EHDX} respectively.

Figure 13. Write Enable Controlled, Write AC Waveforms



Note: 1. During this period DQ0-DQ7 are in output state and input signals should not be applied.

Figure 14. Chip Enable Controlled, Write AC Waveforms

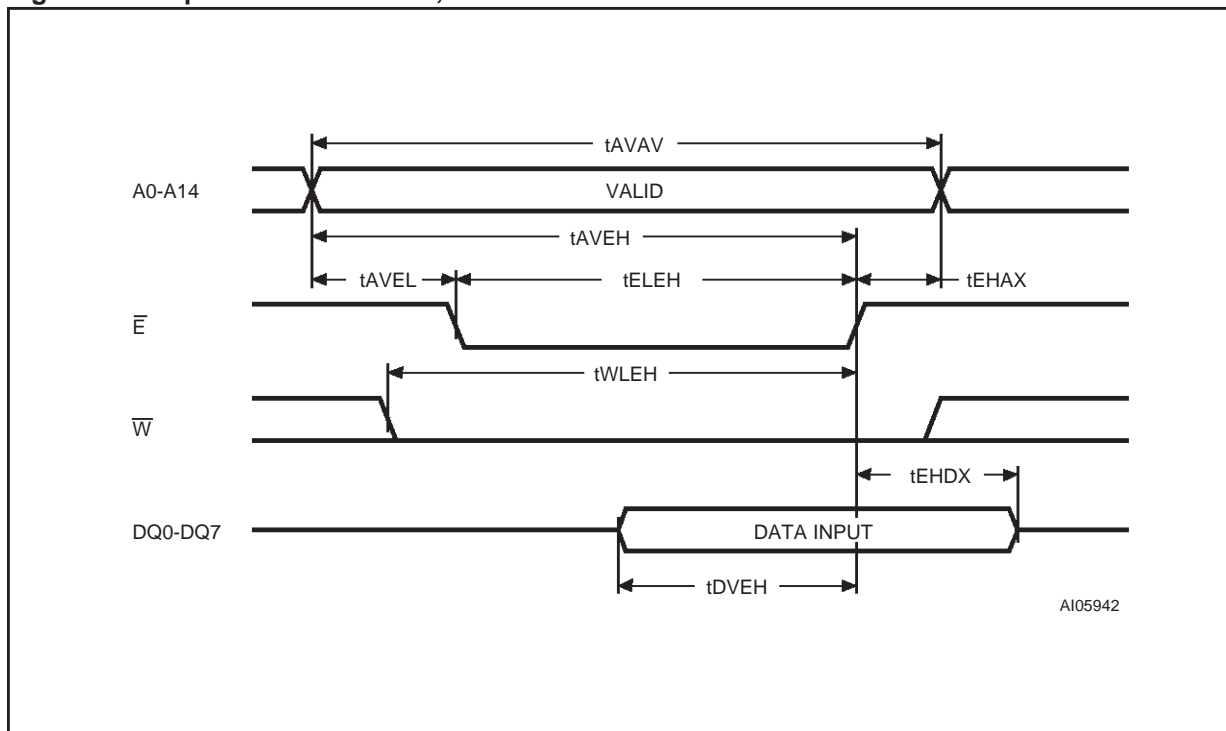


Table 8. Write Mode AC Characteristics

Symbol	Parameter		M68AF031AL	Unit
			70	
t_{AVAV}	Write Cycle Time	Min	70	ns
t_{AVEH}	Address Valid to Chip Enable High	Min	60	ns
t_{AVEL}	Address valid to Chip Enable Low	Min	0	ns
t_{AVWH}	Address Valid to Write Enable High	Min	60	ns
t_{AVWL}	Address Valid to Write Enable Low	Min	0	ns
t_{DVEH}	Input Valid to Chip Enable High	Min	30	ns
t_{DVWH}	Input Valid to Write Enable High	Min	30	ns
t_{EHAX}	Chip Enable High to Address Transition	Min	0	ns
t_{EHDX}	Chip enable High to Input Transition	Min	0	ns
t_{ELEH}	Chip Enable Low to Chip Enable High	Min	60	ns
t_{ELWH}	Chip Enable Low to Write Enable High	Min	60	ns
t_{WHAX}	Write Enable High to Address Transition	Min	0	ns
t_{WHDX}	Write Enable High to Input Transition	Min	0	ns
$t_{WHQX}^{(1)}$	Write Enable High to Output Transition	Min	5	ns
t_{WLEH}	Write Enable Low to Chip Enable High	Min	60	ns
$t_{WLQZ}^{(1,2)}$	Write Enable Low to Output Hi-Z	Max	25	ns
t_{WLWH}	Write Enable Low to Write Enable High	Min	60	ns

Note: 1. At any given temperature and voltage condition, t_{WLQZ} is less than t_{WHQX} for any given device.

2. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 15. Low V_{CC} Data Retention AC Waveforms

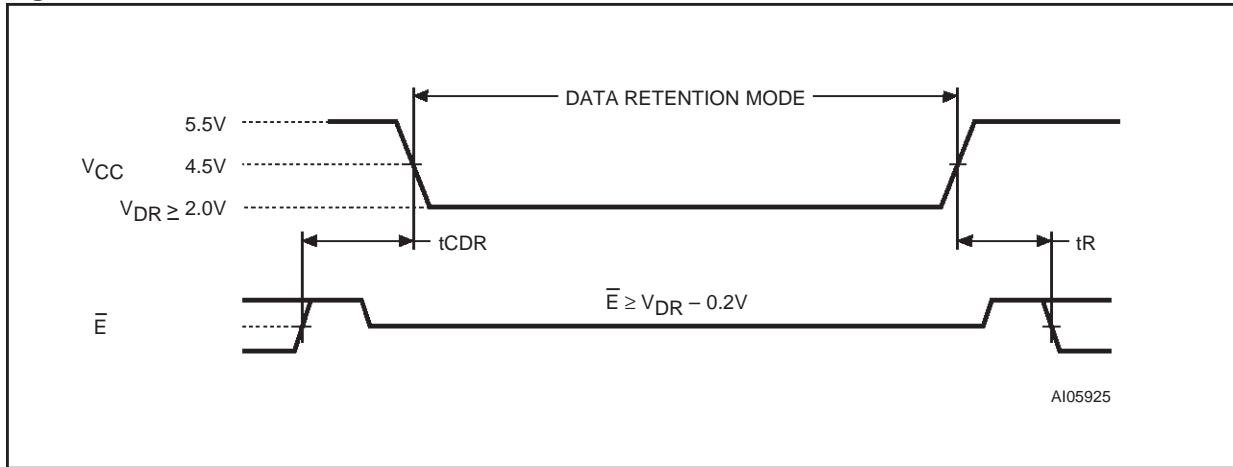


Table 9. Low V_{CC} Data Retention Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I _{CCDR} ⁽¹⁾	Supply Current (Data Retention)	V _{CC} = 2.0V, E-bar ≥ V _{CC} - 0.2V, f = 0 ⁽³⁾			6	μA
t _{CDR} ^(1,2)	Chip Deselected to Data Retention Time		0			ns
t _R ⁽²⁾	Operation Recovery Time		t _{AVAV}			ns
V _{DR} ⁽¹⁾	Supply Voltage (Data Retention)	E-bar ≥ V _{CC} - 0.2V, f = 0	2.0			V

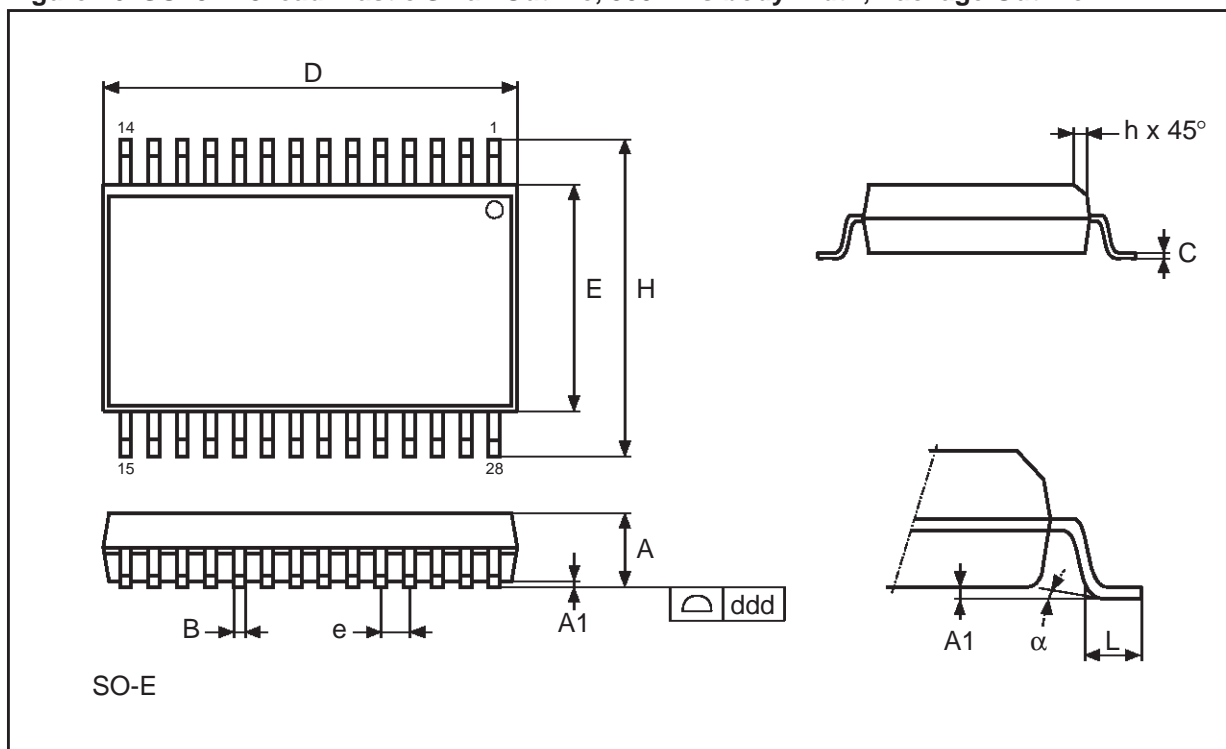
Note: 1. All other Inputs at V_{IH} ≥ V_{CC} - 0.2V or V_{IL} ≤ 0.2V.

2. Tested initially and after any design or process changes that may affect these parameters. t_{AVAV} is Read cycle time.

3. No input may exceed V_{CC} + 0.2V.

PACKAGE MECHANICAL

Figure 16. SO28 - 28 lead Plastic Small Outline, 300 mils body width, Package Outline



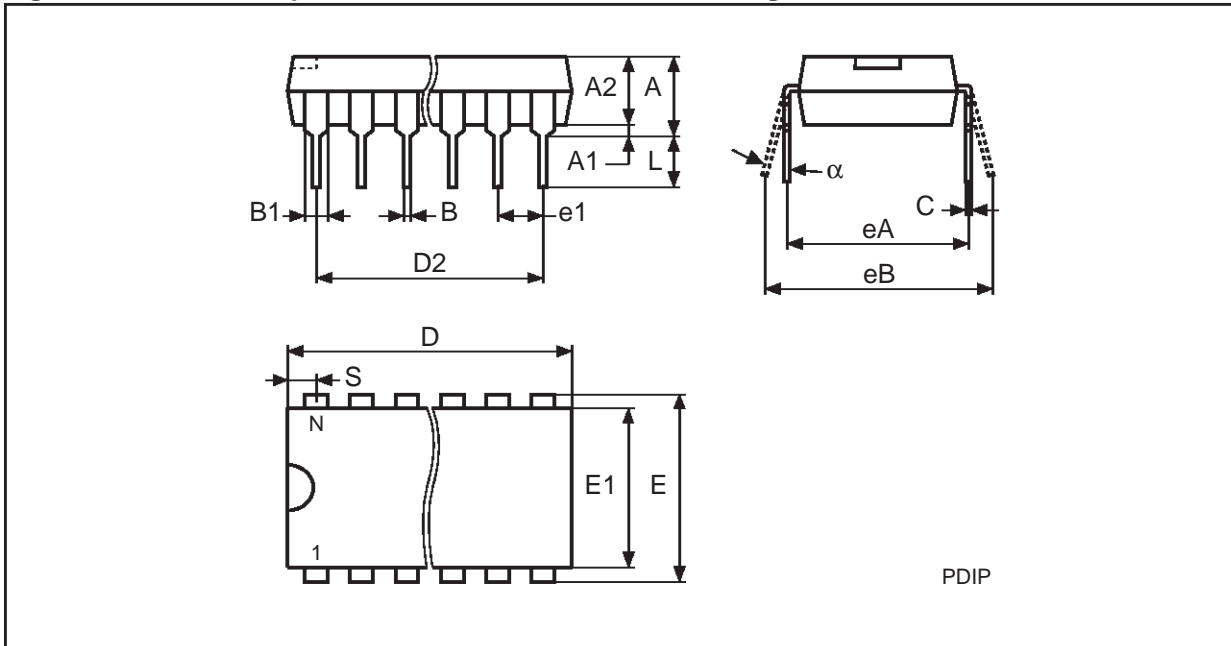
Note: Drawing is not to scale.

Table 10. SO28 - 28 lead Plastic Small Outline, 300 mils body width, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.38	2.79		0.094	0.110
A1		0.05	0.35		0.002	0.014
A2		2.28	2.43		0.090	0.096
B		0.35	0.50		0.014	0.020
C		0.20	0.30		0.008	0.012
D		18.03	18.41		0.710	0.725
ddd			0.10			0.004
E		7.39	7.62		0.291	0.300
e	1.27	–	–	0.050	–	–
H		11.68	12.19		0.460	0.480
L		0.79	1.27		0.031	0.050
α		0°	8°		0°	8°
N		28			28	

M68AF031AL

Figure 17. PDIP28 - 28 pin Plastic DIP, 600 mils width, Package Outline

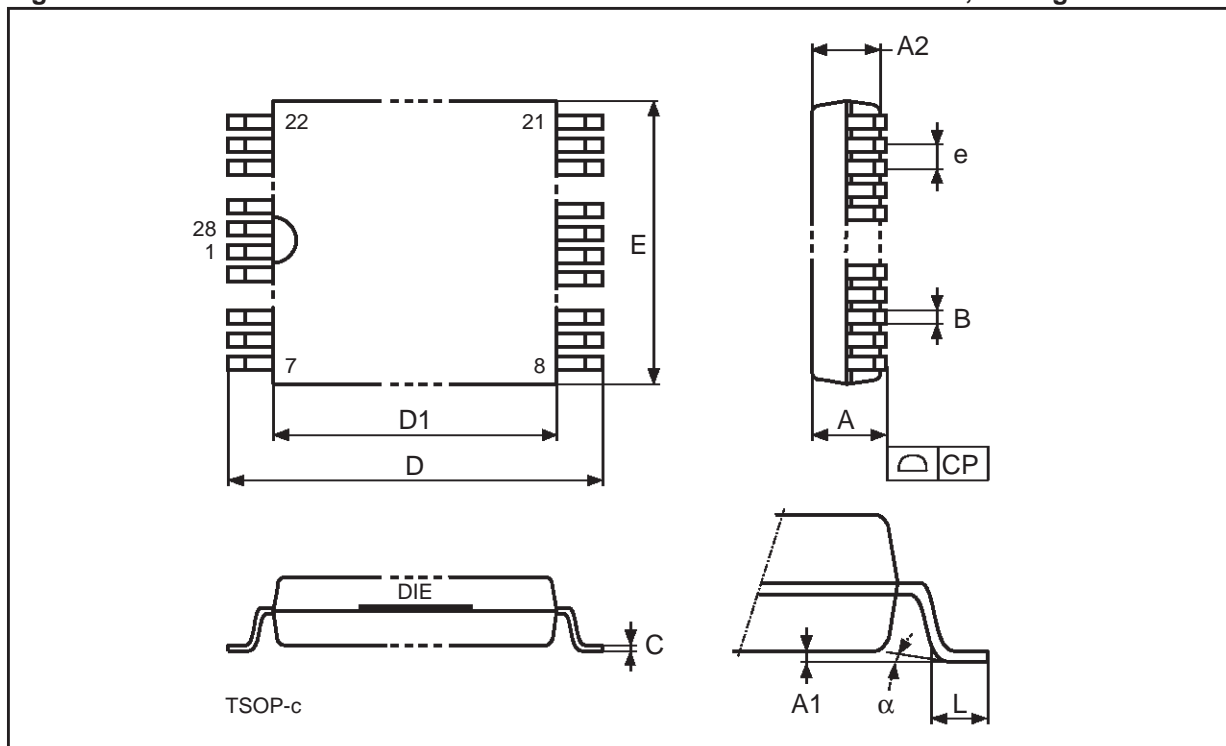


Note: Drawing is not to scale.

Table 11. PDIP28 - 28 pin Plastic DIP, n600 mils width, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		–	5.08		–	0.200
A1		0.38	–		0.015	–
A2		3.56	4.06		0.140	0.160
B		0.38	0.51		0.015	0.020
B1	1.52	–	–	0.060	–	–
C		0.20	0.30		0.008	0.012
D		36.83	37.34		1.450	1.470
D2	33.02	–	–	1.300	–	–
E	15.24	–	–	0.600	–	–
E1		13.59	13.84		0.535	0.545
e1	2.54	–	–	0.100	–	–
eA	14.99	–	–	0.590	–	–
eB		15.24	17.78		0.600	0.700
L		3.18	3.43		0.125	0.135
S		1.78	2.08		0.070	0.082
α		0°	10°		0°	10°
N	28			28		

Figure 18. TSOP28 - 28 lead Normal and Reverse Pinout Plastic Small Outline, Package Outline



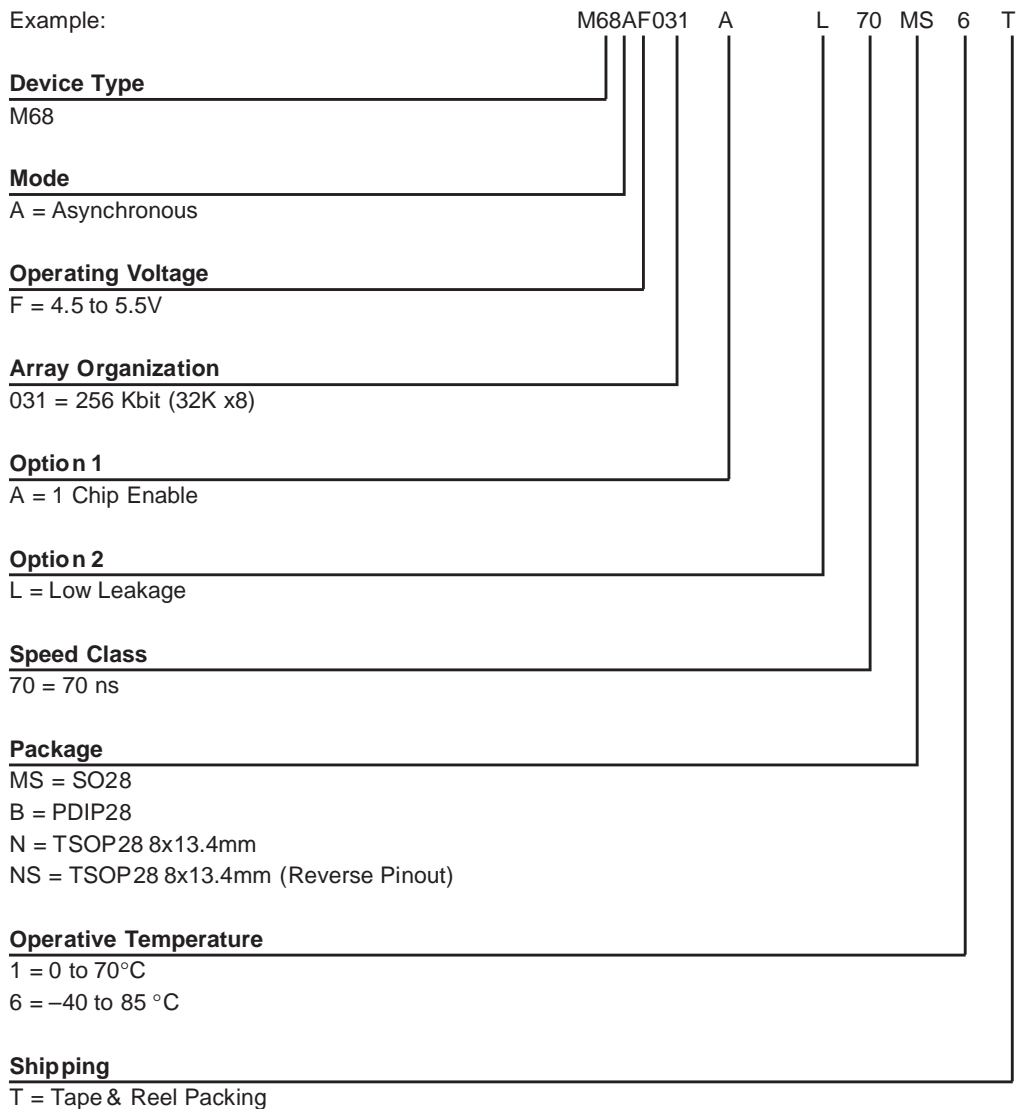
Note: Drawing is not to scale.

Table 12. TSOP28 - 28 lead Normal and Reverse Pinout Plastic Small Outline, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.250			0.0492
A1			0.200			0.0079
A2		0.950	1.150		0.0374	0.0453
B		0.170	0.270		0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.100			0.0039
D		13.200	13.600		0.5197	0.5354
D1		11.700	11.900		0.4606	0.4685
E		7.900	8.100		0.3110	0.3189
e	0.550	–	–	0.0217	–	–
L		0.500	0.700		0.0197	0.0276
α		0°	5°		0°	5°
N		28			28	

PART NUMBERING

Table 13. Ordering Information Scheme



For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

REVISION HISTORY

Table 14. Document Revision History

Date	Version	Revision Details
January 2002	-01	First Issue
07-Feb-2002	-02	I _{SB} clarified
08-Feb-2002	-03	TSOP28 Package removed AC Measurement Load Circuit changed (Figure 9) Operating and AC Measurement Conditions clarified (Table 3)
06-Mar-2002	-04	Document status changed to Data Sheet
19-Apr-2002	-05	Absolute Maximum current value added (Table 2) Operating and AC Measurement Conditions clarified (Table 3)
26-Apr-2002	-06	Absolute Maximum Ratings Table clarified (Table 2) Operating and AC Measurement Conditions Table clarified (Table 3) DC Characteristics Table clarified (Table 5) Write Mode AC Characteristics Table clarified (Table 8) Low V _{CC} Data Retention AC Waveforms clarified (Figure 15) Low V _{CC} Data Retention Characteristics Table clarified (Table 9)
20-May-2002	-07	DC Characteristics Table clarified (Table 5) Low V _{CC} Data Retention Characteristics Table clarified (Table 9)
29-May-2002	-08	TSOP28 8x13.4mm Standard and Reverse pinout added (Figure 1, 5, 6, Table 12)

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